Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	400	interpolat\$3 with phase with quadrature	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR ·	ON	2007/03/20 08:47
L2	14	interpolat\$3 with phase with quadrature with adjust\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 19:43
L3	1	interpolat\$3 with phase with quadrature with adjust\$3 and (eye with diagram)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 09:03
L4	1	((interpolat\$3 with phase with adjust\$3) same quadrature) and (eye with diagram)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 09:03
L5	6	((interpolat\$3 same phase same adjust\$3) same quadrature) and (eye with diagram)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 09:56
L6	2	"4805191".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR .	ON .	2007/03/20 09:54
L7	2	"6731697".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:06

L8		((interpolat\$3 and phase and adjust\$3) and quadrature) and (eye adj diagram)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:54
L9	2	"6,359,878".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 09:59
L10	2	"6,097,794".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:00
L11	2	"5,872,836".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:00
L12	2	"5,065,409".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:07
L13	2	"5,724,413".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:07
L16		(clock adj recovery) with (phase adj interpolator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 11:26

L17	10	(clock adj recovery) with (phase adj interpolator) and quadrature	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:50
L18	12	(clock adj recovery) same (phase adj interpolator) and quadrature	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:50
L19	26	(clock adj recovery) and (phase adj interpolator) and quadrature	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:53
L20	3118	375/371	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:54
L22	3986	375/354	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:54
L23	4027	((interpolat\$3 and phase and adjust\$3) and quadrature)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2007/03/20 10:54
L24	316	interpolator and (phase near3 adjust\$3) and quadrature	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR .	ON	2007/03/20 10:55

L25	84	interpolator same (phase near3 adjust\$3) and quadrature	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:55
L26	19	20 and 25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:55
L27	10	22 and 25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 10:59
L28	23	("4692931" "4815103" "5016206" "5093841" "5202901" "5255289" "5259005" "5283815" "5309482" "5311544" "5343498" "5425057" "5504785").PN. OR ("5602879"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/20 11:13
L29	26	("5386239" "5504785" "5535252" "5610948" "5612975" "5724396" "5793818").PN. OR ("5878088").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/20 11:17
L30	0	("2004/0037366").URPN.	USPAT	OR	ON	2007/03/20 11:24
L31	0	("2004/0037366").URPN.	USPAT	OR	ON	2007/03/20 11:25
L32	47	(clock adj recovery) with (phase with interpolator) and quadrature	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 11:54
L33	56	(clock adj recovery) with (phase adj interpolator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 14:46

L34	1	(clock adj recovery) with (interpolator) with quadrature	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 11:58
L35	9	(clock adj recovery) same (interpolator) same quadrature	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 14:18
L36	3	"6,671,342".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 12:05
L37	23	("4692931" "4815103" "5016206" "5093841" "5202901" "5255289" "5259005" "5283815" "5309482" "5311544" "5343498" "5425057" "5504785").PN. OR ("5602879"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/20 12:45
L38	87	interpolator with correlator	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/20 14:38
L39	37	interpolator with correlator and quadrature	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/20 14:36
L40	1	interpolator with correlator and quadrature and clock adj recovery	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/20 12:47
L41	160	(clock adj recovery) and (interpolator) and quadrature	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 14:18
L42	22	22 and 41	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 14:18

L43	0	interpolator with correlator and pliphase	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/20 14:39
L44	0	interpolator with correlator and pliphaseo	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/20 14:39
L45	10	interpolator with correlator and polyphase	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/20 14:42
L46	0	interpolator with correlator and "poly-phase"	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/20 14:43
L47	8	interpolator and correlator and "poly-phase"	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/20 14:43
L48	120	interpolator with polyphase	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/20 14:48
L49	7	interpolator with polyphase and clock adj recovery	US-PGPUB; USPAT; USOCR	OR	ON	2007/03/20 14:43
L50	8142	chip adj die	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 19:24
L51	2	1 and 50	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 19:25
L52	1	33 and 50	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 19:26
L53	1	41 and 50	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR ·	ON	2007/03/20 19:26

L54	4	23 and 50	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 19:26
L55	1	24 and 50	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 19:27
L56	1	8 and 50	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 19:27
L57	6	(interpolat\$3 with phase with quadrature with adjust\$3).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 19:44
L58	12	(interpolator and phase and quadrature and adjust and "in-phase").clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/20 19:45
S1	1	"10/396118"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/27 08:40
S2	. 1	10/748236	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/19 21:11

drjatorres@gmail.com | Search History | My Account | Sign out

Google

Web Images Video News Maps more »

interpolator phase adjust quadrature "eye diag Search Preferences

Web Results 1 - 10 of about 265 for interpolator phase adjust quadrature "eye diagram". (0.50 seconds)

Programmable phase interpolator adjustment for ideal data eye ... The system of claim 1, wherein the second interpolator adjusts the phase of the quadrature signal to coincide with a predetermined point on an eye diagram. ... www.freepatentsonline.com/20050147194.html - 71k - Cached - Similar pages

Modern with improved timing recovery using equalized data - Patent ... The error signal provides an input to phase locked loop (PLL) 28 which controls ... The equalized quadrature data I and Q are input to interpolator 30 which ... www.freepatentsonline.com/4805191.html - 28k - Cached - Similar pages [More results from www.freepatentsonline.com]

[PDF] A 43-Gb/s Full-Rate Clock Transmitter in 0.18- m SiGe BiCMOS ...

File Format: PDF/Adobe Acrobat

uous **phase interpolation** (PI) between the **quadrature** outputs of. the full-rate clock divide by two is implemented in order to ex-. ternally **adjust** the ... ieeexplore.ieee.org/iel5/4/32287/01506892.pdf - <u>Similar pages</u>

[РDF] A Semi-Digital Delay-Locked Loop Using an Analog-Based Finite ... File Format: PDF/Adobe Acrobat

phase interpolation with 3-b resolution between them. Since, there are four pairs of phases, ... phase selection at the quadrature phase boundaries for the ... ieeexplore.ieee.org/iel5/8920/28239/101109TCSII2004836035.pdf - Similar pages [More results from ieeexplore.ieee.org]

[PDF] Circuits for CMOS High-Speed I / O in Sub-100nm Technologies File Format: PDF/Adobe Acrobat

shows a typical design of the **phase interpolator**. The **phase interpolator** generates the **phase** by forming. a weighted sum of the **quadrature** phases of the ... ietele.oxfordjournals.org/cgi/reprint/E89-C/3/300.pdf - <u>Similar pages</u>

<u>Synchronization :: Using the Libraries (Communications Blockset)</u>

The controller uses the **phase** estimates to determine the interpolating instants that the **interpolator** uses in the next cycle. ...

www.mathworks.com/access/helpdesk/help/toolbox/commblks/ug/fp49500.html - 44k - Cached - Similar pages

[PPT] www.ece.utexas.edu/~bevans/papers/2004/texasInst20...

File Format: Microsoft Powerpoint - View as HTML

Generate **eye diagram** to visualize PAM signal quality ... Carrier detection and **phase adjustment**. Design of receive filter. Probability of error analysis to ... <u>Similar pages</u>

[PDF] WA 17.6: A Variable-Frequency Parallel I/O Interface with Adaptive ...

File Format: PDF/Adobe Acrobat - View as HTML

Adjusting the relative drive strength between two sets of tri-. state inverters enables variable-weight **interpolation**. A **phase-...** www-vlsi.stanford.edu/papers/gyw_isscc_00.pdf - <u>Similar pages</u>

Digital PSK-type demodulator having clock recovery before carrier ...

4 shows the appearance of the eye diagram for a QPSK modulating signal; ... In this case,

the clock 32 has a **phase adjustment** input 34. The values c, cj, ... www.patentstorm.us/patents/5640125-description.html - 43k - <u>Cached</u> - <u>Similar pages</u>

[PDF] A 10-Gb/s CMOS Clock and Data Recovery Circuit With an Analog ... File Format: PDF/Adobe Acrobat - View as HTML Index Terms—Analog quadrature phase interpolator, chip-to- ... Despite the use of an analog PI, the phase adjustment of the ... www.paritycomputing.com/jpdfs/ieee/ssc/jssc/2005040/03mar/0736krei.pdf - Similar pages

Result Page: 1 2 3 4 5 6 7 8 9 10 Next

interpolator phase adjust quadrature Search

Search within results | Language Tools | Search Tips | Dissatisfied? Help us improve

Google Home - Advertising Programs - Business Solutions - About Google

©2007 Google







About Us

Newsroom

Advisory Board

Submit Web Site

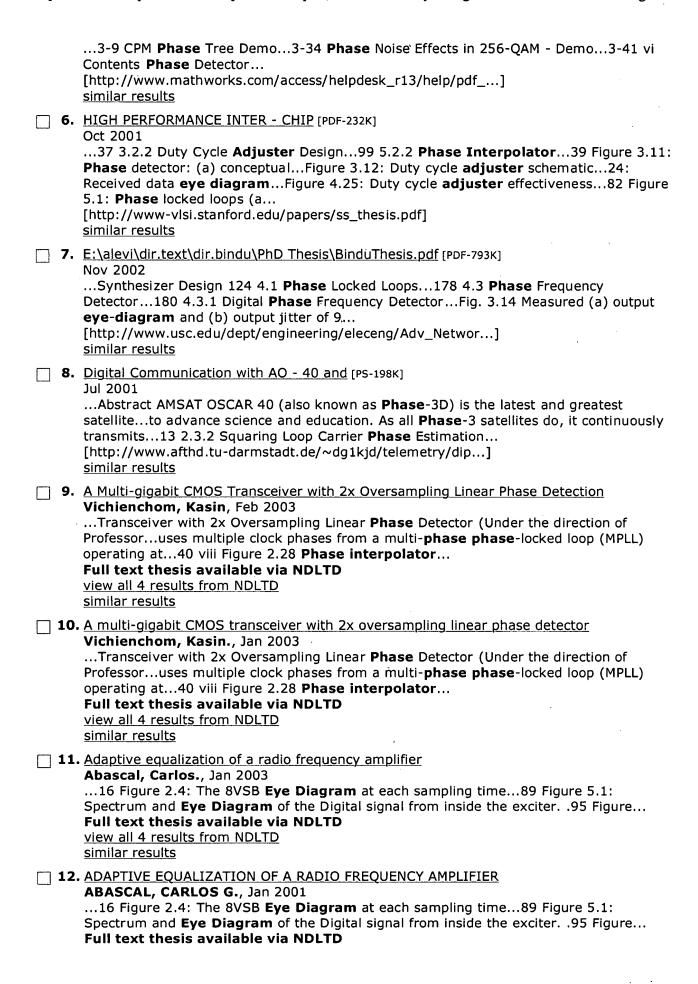
Help

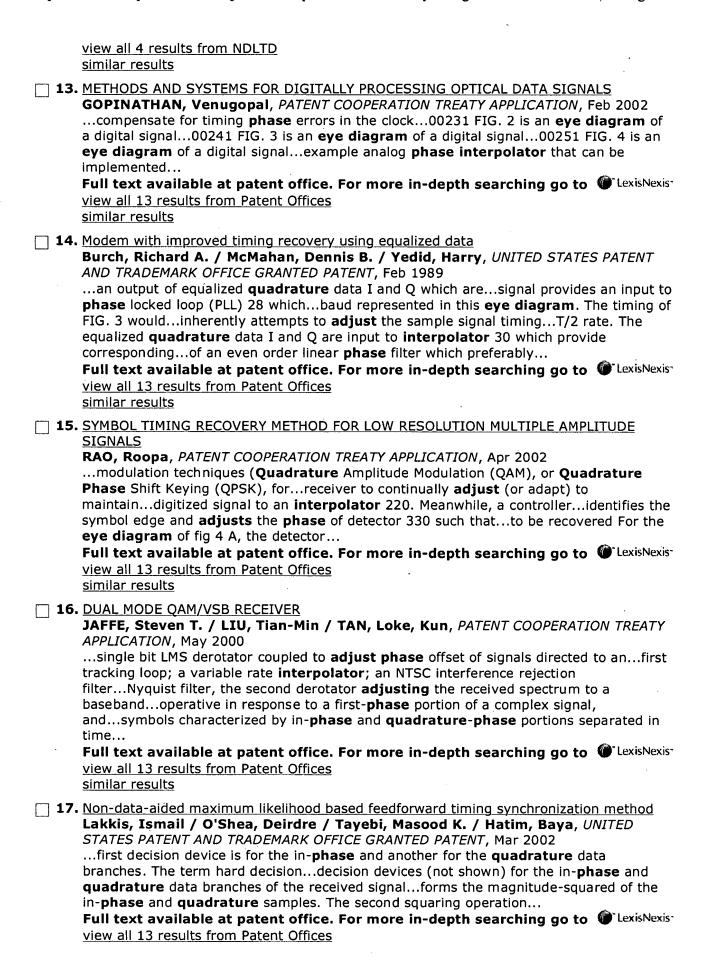
Contact Us

Basic Search

Advanced Search Search Preferences

			interpolator AND phase AND adjust AND quadrature AI Search	
			✓ Journal sources ✓ Preferred Web sources ✓ Other Web sources ☐ Exact phrase	
	Sear	ched for::	:All of the words:interpolator AND phase AND adjust AND quadrature AND "eye diagram	m"
		Found::	:34 total 0 journal results 17 preferred web results 17 other web results	
		Sort by::	:relevance date	
	·····	Save che	cked results Email checked results Export checked results	Re
	1.	No Title [F		us fo
		Nov 2003	aneous frequency of the VCO is adjusted to align the phase of the VCO output	an
		with the p	phase oferror - ^ . Two approaches to carrier phase synchronization can be	an
		envisione	d. In the first approach, phase compensation is performed at the outputfilter ted in Figure 3.7. The quadrature sinusoids used for downconversion are	<u>co</u>
		[http://w	ww.ee.byu.edu/class/ee485public/ee485.fall.03/]	da
		similar re		dig
	2.		<u>ok</u> [PDF-307K]	co eq
		May 2002		fir
				ou
			Self-biased replica-feedback circuit dynamically adjusts the bias voltages of	pe
		•	netric-load <u>from</u> [http://mos.stanford.edu/papers/ey_thesis.pdf]	ph
		similar re		ро
F	3.	thesis.boo	<u>ok</u> [PDF-307K]	rin
		May 2002		SW
			1 Low-Frequency Dynamic Phase Noise Tracking Loop83 ase Noise Measurements19 Figure 2.4: Phase -locked loops: (a) VCO based	01
			Self-biased replica-feedback circuit dynamically adjusts the bias voltages of	Α
		•	netric-load	
		similar re	<u>from</u> [http://velox.stanford.edu/papers/ey_thesis.pdf] sults	
	4.		Communications Blockset [PDF-354K]	
		Jun 2002	•	
			M Phase Tree Demo3-34 Phase Noise Effects in 256-QAM - Demo3-41 vi Phase Detector	
			tila.sdsu.edu/matlab/pdf_doc/commblks/usersgu]	
		similar re		
	5.	Using the	Communications Blockset [PDF-354K]	





	similar results
18.	Host computer digital signal processing system for communicating over voice-grade telephone channels Suffern, Robert C. / Norrell, Andrew L., UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Aug 2000 values from the interface card and performs band-splitting and phase-splitting digital filtering to create filtered samples forthe host computer's screen to provide an oscilloscope-like eye-diagram display useful for monitoring the performance of the system Full text available at patent office. For more in-depth searching go to View all 13 results from Patent Offices similar results
19.	ALIGNMENT METHOD AND APPARATUS FOR RETRIEVING INFORMATION FROM A TWO-DIMENSIONAL DATA ARRAY LAYBOURN, Loren / BLAHUT, Richard E. / RUSSELL, James T., PATENT COOPERATION TREATY APPLICATION, Nov 1997 generation of polynomials, make use of in-phase and quadrature spatial reference signals to modulatethis manner, the combination of in-phase and quadrature spatial reference signals generatesindependent measure of the timing signal phase as a function of position along the Full text available at patent office. For more in-depth searching go to view all 13 results from Patent Offices similar results
_ 20.	Host computer digital signal processing system for communicating over voice-grade telephone channels Suffern, Robert C. / Norrell, Andrew L., UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Feb 1999 values from the interface card and performs band-splitting and phase-splitting digital filtering to create filtered samples forthe host computer's screen to provide an oscilloscope-like eye-diagram display useful for monitoring the performance of the system Full text available at natent office. For more in-depth searching go to

:::fast

Results Pages: [<< Prev] 1 2 [Next >>]

view all 13 results from Patent Offices

similar results

back to top

<u>Downloads</u> | <u>Subscribe to News Updates</u> | <u>User Feedback</u> | <u>Advertising</u> <u>Tell A Friend</u> | <u>Terms Of Service</u> | <u>Privacy Policy</u> | <u>Legal</u>

Powered by FAST © Elsevier 2007

SCIFUS for scientific information only



About Us

Newsroom

Advisory Board

Submit Web Site

Help

Contact Us

Basic	Search Advanced Search Preferences	
	Interpolator AND phase AND adjust AND quadrature AI Search ✓ Journal sources ✓ Preferred Web sources ✓ Other Web sources □ Exact phrase	
Searched for:: Found:: Sort by::	:All of the words:interpolator AND phase AND adjust AND quadrature AND "eye diagram :34 total 0 journal results <u>17 preferred web results</u> <u>17 other web results</u> :relevance <u>date</u>	n'
21. FSK disc Hughes TRADEM mutua quadrat illustrate Full tex	Reprint the series of the seri	Re us for arranged disconnections of the connection of the connect
EUROPEusuallipairs are the eye interpola	AN PATENT, Mar 1989 y in a continuous phase manner. The generalof the FIR filter, quadrature used withillustrates a typical eye diagram; Figures 5a to 5cillustrated in diagram of figure 4. In orderoption is to employ an interpolator 22 which atesprovides the necessary phase quadrature frequency discrimination t available at patent office. For more in-depth searching go to LexisNexistanties.	fir OL pe ph pr rir SV
HUGHE: PATENTmutua - Figure: 4to er carried of frequence Full tex	CRIMINATOR S, Patrick, Michael / HALL, Martin, Christopher / LIND, Larry, Frederick, COOPERATION TREATY APPLICATION, Feb 1989 ally in phase quadrature, at the keyingillustrates a typical eye diagram; andthe signal phase at the intersymbolillustrated in the eye diagram of figure inploy an interpolator 22 which interpolatesIk-4. 51 The interpolator 6 butiteratively adjusted, as followsthe necessary phase quadrature by discrimination t available at patent office. For more in-depth searching go to LexisNexis 13 results from Patent Offices	
	nputer digital signal processing system for communicating over voice-grade	

		OFFICE GRANTED PATENT, Mar 1998
		values from the interface card and performs band-splitting and phase -splitting digital
		filtering to create filtered samples forthe host computer's screen to provide an
		oscilloscope-like eye-diagram display useful for monitoring the performance of the
		system
		Full text available at patent office. For more in-depth searching go to LexisNexis-
		view all 13 results from Patent Offices
		<u>similar results</u>
	25	Host computer digital signal processing system for communicating over voice-grade
	29.	telephone channels
		Suffern, Robert C. / Norrell, Andrew L., UNITED STATES PATENT AND TRADEMARK
		OFFICE GRANTED PATENT, Jul 1997
		values from the interface card and performs band-splitting and phase -splitting digital
		filtering to create filtered samples forthe host computer's screen to provide an
		oscilloscope-like eye-diagram display useful for monitoring the performance of the
		system
		Full text available at patent office. For more in-depth searching go to LexisNexis
		<u>view all 13 results from Patent Offices</u> <u>similar results</u>
	26.	HIGH PERFORMANCE INTER - CHIP [PDF-248K]
		Oct 2001
		37 3.2.2 Duty Cycle Adjuster Design99 5.2.2 Phase Interpolator 39 Figure 3.11:
		Phase detector: (a) conceptualFigure 3.12: Duty cycle adjuster schematic24: Received data eye diagram Figure 4.25: Duty cycle adjuster effectiveness82 Figure
		5.1: Phase locked loops (a
		[http://mos.stanford.edu/papers/ss_thesis.pdf]
		similar results
Г	27.	HIGH PERFORMANCE INTER - CHIP [PDF-249K]
L		Oct 2001
		37 3.2.2 Duty Cycle Adjuster Design99 5.2.2 Phase Interpolator 39 Figure 3.11:
		Phase detector: (a) conceptualFigure 3.12: Duty cycle adjuster schematic24:
		Received data eye diagram Figure 4.25: Duty cycle adjuster effectiveness82 Figure
		5.1: Phase locked loops (a
		[http://velox.stanford.edu/papers/ss_thesis.pdf] similar_results
	28.	Design of CMOS Adaptive-Supply Serial Links [PDF-271K]
		Dec 2002
		21 2.2.1 Phase Portrait AnalysisMajority-voting for decimating multiple phase detector outputs: (a) circuit87 4.17 Digital phase interpolator 7V 96 5.5
		Transmitter eye diagram of the adaptive-supply serial
		[http://velox.stanford.edu/papers/jk_thesis.pdf]
		similar results
\Box	29.	Design of CMOS Adaptive-Supply Serial Links [PDF-271K]
L)		Dec 2002
		21 2.2.1 Phase Portrait AnalysisMajority-voting for decimating multiple phase
		detector outputs: (a) circuit87 4.17 Digital phase interpolator 7V 96 5.5
		Transmitter eye diagram of the adaptive-supply serial
		[http://mos.stanford.edu/papers/jk_thesis.pdf] similar_results
	_	
	30.	Data Converters for High Speed CMOS Links [PDF-191K]
		Oct 2001 51.4.4.1 Digital Phase Detector 11 Figure 2.7: PLL Phase Noise Spectrum 13
		51 4.4.1 Digital Phase Detector11 Figure 2.7: PLL Phase Noise Spectrum13 Figure 2.9: Clock Interpolator 67 Figure 5.5: PLL Phase Noise vs. Noise Frequency

	[http://velox.stanford.edu/papers/wfe_thesis.pdf] similar results
□ 31.	Data Converters for High Speed CMOS Links [PDF-190K] Oct 200151 4.4.1 Digital Phase Detector11 Figure 2.7: PLL Phase Noise Spectrum13 Figure 2.9: Clock Interpolator 67 Figure 5.5: PLL Phase Noise vs. Noise Frequency [http://mos.stanford.edu/papers/wfe_thesis.pdf] similar results
□ 32.	thesis.book [PDF-238K] Sep 200172 Figure 4.12. Phase -only detector74 Figure 4.13. Phase detector transient waveforms93 Figure 4.27. Phase interpolation95 Figure 4.28. Digital interpolator96 Figure 4.30. Duty-cycle adjuster schematic [http://mos.stanford.edu/papers/gyw_thesis.pdf] similar results
□ 33.	thesis.book [PDF-238K] Sep 200172 Figure 4.12. Phase -only detector74 Figure 4.13. Phase detector transient waveforms93 Figure 4.27. Phase interpolation95 Figure 4.28. Digital interpolator96 Figure 4.30. Duty-cycle adjuster schematic [http://velox.stanford.edu/papers/gyw_thesis.pdf] similar results
□ 34.	Data Converters for High Speed CMOS Links [PDF-185K] Oct 2001nonlinearity, clock coupling, and static phase errors are also digitally corrected. Time51 4.4.1 Digital Phase Detector67 Figure 5.5: PLL Phase Noise vs. Noise Frequency [http://velox.stanford.edu/~bellersi/thesis.pdf] similar results
	:::fast

Results Pages: [<< Prev] 1 2 [Next >>]

back to top

Powered by FAST © Elsevier 2007



Home | Login | Logout | Access Information | Alerts |

Welcome United States Patent and Trademark Office

Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "(((interpolator<in>metadata) <and> (eye diagram<in>metadata))) <and> (..."

Your search matched 0 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

View Session History

Modify Search

New Search

(((interpolator<in>metadata) <and>(eye diagram<in>metadata))) <and>(pyr >=

Search

☑ e-mail

Check to search only within this results set

» Key

IET JNL.

IET CNF

Display Format: © Citation © Citation & Abstract

IEEE Journal or **IEEE JNL**

Magazine

IET Journal or Magazine

IEEE CNF IEEE Conference

Proceeding

IET Conference

Proceeding

No results were found.

Please edit your search criteria and try again. Refer to the Help pages if you need assistan

IEEE STD IEEE Standard

Help Contact Us Privacy &:

© Copyright 2006 IEEE -

Indexed by ig inspec



Home | Login | Logout | Access Information | Alerts |

Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "((interpolator<in>metadata) <and> (quadrature<in>metadata))"

Your search matched 24 of 1520067 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

⊠ e-mail

» Search Options

View Session History

New Search

» Key

IEEE JNL IEE

IEEE Journal or

Magazine

IET JNL

IET Journal or Magazine

IEEE CNF

IEEE Conference Proceeding

IET CNF

IET Conference

Proceeding

IEEE STD IEEE Standard

Modify Search

((interpolator<in>metadata) <and> (quadrature<in>metadata))

Search

Check to search only within this results set

•

ر view selected items ا

Select All Deselect All

1. A double Nyquist digital product detector for quadrature sampling

Pellon, L.E.;

Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on [see also Acoustics, IEEE T

IEEE Transactions on]

Volume 40, Issue 7, July 1992 Page(s):1670 - 1681

Digital Object Identifier 10.1109/78.143439

AbstractPlus | Full Text: PDF(1012 KB) | IEEE JNL

Rights and Permissions

2. A high-resolution interpolator for incremental encoders based on the qua

Emura, T.; Lei Wang;

Industrial Electronics, IEEE Transactions on

Volume 47, Issue 1, Feb. 2000 Page(s):84 - 90

Digital Object Identifier 10.1109/41.824129

AbstractPlus | References | Full Text: PDF(204 KB) IEEE JNL

Rights and Permissions

3. Optimization of PSAM for diversity 16-QAM

Lingzhi Cao; Beaulieu, N.C.;

Wireless Communications and Networking Conference, 2004. WCNC. 2004 IE

Volume 2, 21-25 March 2004 Page(s):1171 - 1174 Vol.2

AbstractPlus | Full Text: PDF(276 KB) | IEEE CNF

Rights and Permissions

4. Comparative study of pilot symbol assisted modem schemes

Torrance, J.M.; Hanzo, L.;

Radio Receivers and Associated Systems, 1995., Sixth International Conferen-

26-27 Sep 1995 Page(s):36 - 41

AbstractPlus | Full Text: PDF(464 KB) IET CNF

5. Exact BERs for M-QAM with MRC and channel estimation errors in Rician

Yao Ma; Schober, R.; Dongbo Zhang;

Wireless Communications and Networking Conference, 2005 IEEE

Volume 2, 13-17 March 2005 Page(s):967 - 972 Vol. 2

Digital Object Identifier 10.1109/WCNC.2005.1424639

AbstractPlus | Full Text: PDF(1844 KB) | IEEE CNF

Rights and Permissions

6. Structural subband decomposition: a new concept in digital signal proce Mitra, S.K.;

> Image and Signal Processing and Analysis, 2001, ISPA 2001, Proceedings of International Symposium on

19-21 June 2001 Page(s):2

Digital Object Identifier 10.1109/ISPA.2001.938595

AbstractPlus | Full Text: PDF(28 KB) | IEEE CNF

Rights and Permissions

7. A VLSI architecture for a frequency-agile single-chip 10-MBaud digital QA

Kyung-Ho Cho; Putnam, J.; Samueli, H.;

Global Telecommunications Conference, 1999. GLOBECOM '99

Volume 1A, 1999 Page(s):168 - 172 vol.1a

Digital Object Identifier 10.1109/GLOCOM.1999.831629

AbstractPlus | Full Text: PDF(360 KB) IEEE CNF

Rights and Permissions

8. A new timing recovery method for DTV receivers

Bao, J.; Lu, C.Y.; Da Graca, P.; Zeng, S.; Poon, T.;

Consumer Electronics, IEEE Transactions on

Volume 44, Issue 4, Nov. 1998 Page(s):1243 - 1249 Digital Object Identifier 10.1109/30.735823

AbstractPlus | Full Text: PDF(436 KB) | IEEE JNL

Rights and Permissions

9. Performance of an adaptive rate modem using quasi-analytic simulation t

Wickert, M.A.; Hofstetter, P.;

Microwave Theory and Techniques, IEEE Transactions on

Volume 47, Issue 6, Part 1, June 1999 Page(s):687 - 692

Digital Object Identifier 10.1109/22.769336

AbstractPlus | References | Full Text: PDF(168 KB) | IEEE JNL

Rights and Permissions

10. Implementation of a real-time frequency-selective RF channel simulator (DSP-FPGA architecture

Wickert, M.A.; Papenfuss, J.;

Microwave Theory and Techniques, IEEE Transactions on

Volume 49, Issue 8, Aug. 2001 Page(s):1390 - 1397

Digital Object Identifier 10.1109/22.939918

AbstractPlus | References | Full Text: PDF(168 KB) | IEEE JNL

Rights and Permissions

11. A 10-gb/s CMOS clock and data recovery circuit with an analog phase int Г

Kreienkamp, R.; Langmann, U.; Zimmermann, C.; Aoyama, T.; Siedhoff, H.;

Solid-State Circuits, IEEE Journal of

Volume 40, Issue 3, March 2005 Page(s):736 - 743

Digital Object Identifier 10.1109/JSSC.2005.843624

AbstractPlus | References | Full Text: PDF(616 KB) | IEEE JNL

Rights and Permissions

12. Design of a QPSK/16 QAM LMDS downstream receiver ASIC chip

Park, K.H.; Shin, D.K.; Lee, J.S.; Sunwoo, M.H.;

Signal Processing Systems, 2000. SiPS 2000. 2000 IEEE Workshop on

11-13 Oct. 2000 Page(s):210 - 217

Digital Object Identifier 10.1109/SIPS.2000.886718

AbstractPlus | Full Text: PDF(316 KB) IEEE CNF

Rights and Permissions

Г 13. A QPSK/16 QAM receiver chip for LMDS application

Ki Hyuk Park; Dae Kyo Shin; Jun Sung Lee; Sunwoo, M.H.;

ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Co

28-30 Aug. 2000 Page(s):207 - 210

Digital Object Identifier 10.1109/APASIC.2000.896945

AbstractPlus | Full Text: PDF(248 KB) | IEEE CNF

Rights and Permissions

14. Symbol-timing recovery for M-PSK modulation schemes using the signul

Verdin, D.; Tozer, T.C.;

New Synchronisation Techniques for Radio Systems, IEE Colloquium on

27 Nov 1995 Page(s):2/1 - 2/7

AbstractPlus | Full Text: PDF(292 KB) IET CNF

15. Interpolator for all-digital receivers

Zhang, H.;

Electronics Letters

Volume 33, Issue 4, 13 Feb. 1997 Page(s):261 - 262

AbstractPlus | Full Text: PDF(236 KB) IET JNL

16. Optimal design and simulation for multi-rate symbol timing recovery in s ___ **QPSK** demodulation

Hao Wei; Shen Ming; Zhao Hui;

Computational Electromagnetics and Its Applications, 2004. Proceedings. ICC

3rd International Conference on

1-4 Nov. 2004 Page(s):312 - 315

Digital Object Identifier 10.1109/ICCEA.2004.1459354

AbstractPlus | Full Text: PDF(182 KB) | IEEE CNF

Rights and Permissions

17. Multiplierless multirate decimator/interpolator module generator Г

Shyh-Jye Jou; Kai-Yuan Jheng; Hsiao-Yun Chen; An-Yeu Wu;

Advanced System Integrated Circuits 2004. Proceedings of 2004 IEEE Asia-P.

4-5 Aug. 2004 Page(s):58 - 61

Digital Object Identifier 10.1109/APASIC.2004.1349404

AbstractPlus | Full Text: PDF(370 KB) | IEEE CNF

Rights and Permissions

18. Farrow structure interpolators based on even order shaped Lagrange pol

Ghadam, A.S.H.; Renfors, M.;

Image and Signal Processing and Analysis, 2003. ISPA 2003. Proceedings of

International Symposium on

Volume 2, 18-20 Sept. 2003 Page(s):745 - 748 Vol.2

Digital Object Identifier 10.1109/ISPA.2003.1296375

AbstractPlus | Full Text: PDF(1373 KB) IEEE CNF

Rights and Permissions

19. Fast symbol timing recovery techniques for flexible PAM and QAM mode

Vo, N.D.; Le-Ngoc, T.;

Electrical and Computer Engineering, 2003. IEEE CCECE 2003. Canadian Co

Volume 3, 4-7 May 2003 Page(s):1959 - 1962 vol.3

AbstractPlus | Full Text: PDF(287 KB) | IEEE CNF

Rights and Permissions

Pilot-symbol assisted channel estimation for coherent DS-CDMA commu

Hai-Wei Wang; Che-Ho Wei;

Circuits and Systems, 2000. Proceedings, ISCAS 2000 Geneva. The 2000 IEE Symposium on

Volume 3, 28-31 May 2000 Page(s):383 - 386 vol.3 Digital Object Identifier 10.1109/ISCAS.2000.856077

AbstractPlus | Full Text: PDF(256 KB) IEEE CNF Rights and Permissions

21. Channel estimation for the W-CDMA system, performance and robustnes Г a terminal perspective

Lindoff, B.; Ostberg, C.; Eriksson, H.;

Vehicular Technology Conference, 1999 IEEE 49th

Volume 2, 16-20 May 1999 Page(s):1565 - 1569 vol.2 Digital Object Identifier 10.1109/VETEC.1999.780649

AbstractPlus | Full Text: PDF(356 KB) | IEEE CNF

Rights and Permissions

22. Effect of frequency offset on carrier phase and symbol timing recovery ir receivers

Hamila, R.; Vesma, J.; Vuolle, H.; Renfors, M.;

Signals, Systems, and Electronics, 1998. ISSSE 98. 1998 URSI International 5

29 Sept.-2 Oct. 1998 Page(s):247 - 252

Digital Object Identifier 10.1109/ISSSE.1998.738075

AbstractPlus | Full Text: PDF(400 KB) | IEEE CNF

Rights and Permissions

23. New Rayleigh fading channel estimator based on PSAM channel soundin Г Young-Su Kim; Chang-Joo Kim; Goo-Young Jeong; Young-Jo Bang; Han-Kyu

Choi:

Communications, 1997. ICC 97 Montreal, 'Towards the Knowledge Millennium International Conference on

Volume 3, 8-12 June 1997 Page(s):1518 - 1520 vol.3

Digital Object Identifier 10.1109/ICC.1997.595042

AbstractPlus | Full Text: PDF(180 KB) | IEEE CNF

Rights and Permissions

24. VLSI implementation of on board processing subsystems for satellite characteristics. Г

Jamali, M.M.; Kwatra, S.C.;

Circuits and Systems, 1996., IEEE 39th Midwest symposium on

Volume 3, 18-21 Aug. 1996 Page(s):1235 - 1238 vol.3

Digital Object Identifier 10.1109/MWSCAS.1996.593132

AbstractPlus | Full Text: PDF(264 KB) | IEEE CNF

Rights and Permissions

Help Contact Us Privacy &:

© Copyright 2006 IEEE -

indexed by Inspec



Newsroom

About Us

scirus 🔩	Sear	ch) 🕶 🛭 🛭	Pop-up Blocker (OFF / Highlight
lvisory Board	Submit Web Site	Help	!	Contact Us

	Basic Search	Advanced Search Preferences			
	•	" AND interpolator AND quadrature Search ✓ Preferred Web sources ✓ Other Web sources □ Exact phrase			
S		ds:"clock recovery" AND interpolator AND quadrature journal results 106 preferred web results 28 other web results date			
1.	Save checked results Adaptive supply serial link State Circuits, IEEE Journa Mar 2003	Email checked results Export checked results s with sub-1-V operation and per-pin clock recovery - Solid- al of [PDF-53K]	Dic "cli int qu		
	b-1-V Operation and Per supply regulation, clock re clock recovery since they interpolators [38][41]. F	r-Pin Clock Recovery Jaeha Kim, Student Memberpower-ecovery phase/delay-locked loopneed per-pin multiphase may be connectedopen-loop fashion using delay for these techniques s.stanford.edu/papers/jk_jssc0211.pdf]	Re us for and cor aut		
2.	network ICs - Solid-State Apr 2003part. The clock recover overcometraditional ana power consumptionProp phase mixing interpolato	le 2.5-3.125-Gb/s serial link macrocellfor high IO bandwidth Circuits, IEEE [PDF-34K] ry is based onanalog phase interpolator to log quadrature-phase mixingcases. The interpolator's osed Clock Recovery Loop A particularity of the quadrature r is that itsignals. The clock recovery loop, however n/~rodoni/download/local_paper]	clo cor cut dat dig fur fur		
3.	interpolators5.11: Sim	lator5.10: Timing generation using phase applified model of the phase interpolator ox.stanford.edu/papers/ss_thesis.pdf]	inc int int out ref		
4.	interpolators5.11: Sim	lator5.10: Timing generation using phase applified model of the phase interpolator w-vlsi.stanford.edu/papers/ss_thesis.pdf]	sar Or Al		
<u> </u>	System Parameters [4K] Sep 1995	·			

	phase rotations, perfect carrier and clock recovery were assumed. In case of the linear interpolator the system delay was minimised, sinceshift keying (QPSK) and 16-level quadrature amplitude modulation (16QAM). Theschemes were combined with all four interpolators and their bit error rate (BER) performance [http://www-mobile.ecs.soton.ac.uk/jeff/papers/bath21/n] similar results
6.	HotI97.fm [PDF-42K] May 1998delay stages. The interpolator adjusts the phaseand initializes the interpolator at mid-range. FigureDelay-Locked Loop Tracking Clock Recovery for 4Gb/s Signalingalternative to the tracking clock recovery described above. An [http://www.cs.unc.edu/~jp/HotI97.pdf] similar results
7.	TDA10021HT_4 [PDF-41K] May 2003receiver TDA10021HT FEATURES · 4, 16, 32, 64, 128 and 256 Quadrature Amplitude Modulation (QAM) demodulator (DVB-C compatiblebe BLOCK DIA GRAM handbook, full pagewidth MGW343 CLOCK RECOVERY I2 C-BUS INTERFACE GPIO AGC PWM PWM TIMING INTERPOLATOR RS DECODER OUTPUT INTERFACE JTAG DE-SCRAMBLER DE- INTERLEAVER more hits from [http://www.semiconductors.philips.com/acrobat_download] similar results
8.	E:\alevi\dir.text\dir.bindu\PhD Thesis\BinduThesis.pdf [PDF-793K] Nov 2002 He has been the ideal advisor in providing the environment and the facilities that have made this work possible. His demand for excellence, insight, and suggestions have shaped many of my ideas, and made this dissertation possible. [http://www.usc.edu/dept/engineering/eleceng/Adv_Networ] similar results
9.	Reference-based dual switch and stay diversity systems over correlated Nakagami fading channels - Vehicular Technology, IEEE [PDF-58K] Sep 2003pilot extraction/interpolation filter. Assuming a perfect clock recovery and that satisfies Nyquist's criterion for zero intersymboldenotes the variance of that depends on the type of filter/interpolator used for the pilot reference recovery, represents thechange of variables enables us to use the GaussChebyshev quadrature rules [20, 25.4.38], which have the advantage that their [http://dmi.uib.es/~dmigfn1/recerca/articles/tvtjuly03] similar results
10.	Digital Communication with AO - 40 and [PS-198K] Jul 200178 3.4.4 Downconversion and Costas Loop
11.	McNEILL: JITTER IN PHASE - LOCKED LOOPS [PDF-48K] Apr 2003Theory ·Original application: PLL clock recovery in SONET ·Example of jitter (timeto Transmit Clock RCLK RDATA TDATA CLOCK RECOVERY PLL (D.U.T) TCLK DATA SOURCE COMMUNICATIONSto Transmit Clock RCLK RDATA TDATA CLOCK RECOVERY PLL (D.U.T) TCLK DATA SOURCE COMMUNICATIONS [http://www.ece.wpi.edu/Research/Analog/Resources/pllji] similar results

<u> </u>	Multi-channel serdes receiver for chip-to-chip and backplane interconnects and method of operation thereof
	Yang, Fuji / Larsson, Patrick / O'Neill, Jay, UNITED STATES PATENT AND TRADEMARK OFFICE PRE-GRANT PUBLICATION, Mar 2003provided to the phase interpolator 110 along with the in-phase and quadrature phase signals, I andplurality including a clock recovery system having a phase detector and a phase interpolator, the clock recovery system coupling the Full text available at patent office. For more in-depth searching go to LexisNexis view all 101 results from Patent Offices similar results
13.	Method for equalization of a quadrature amplitude modulated signal Copeland, Gregory Clark, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, May 2000 synchronization and/or clock recovery operations, asoperation, an analog quadrature amplitude modulatedalso includes clock recovery circuit 503 anddemodulator 508, an interpolator and rate conversionand Hanzo, Modem Quadrature Amplitude Modulationof carrier and clock recovery from QAM signals
	Full text available at patent office. For more in-depth searching go to View all 101 results from Patent Offices similar results
14.	Phase synchronisation device and phase quadrature signal generating apparatus Pickering, Andrew James / Joy, Andrew Keith / Simpson, Susan Mary, EUROPEAN PATENT APPLICATION, Apr 1999
	apparatus for generating an output pair of quadrature related signals oscillating at a commonprovides said output signals. The quadrature related signals are advantageouslyand means arranged to regenerate the quadrature relationship between the clock signalsexample implementation of the phase interpolator of Figure 4; Figure 6 is a schematic
	Full text available at patent office. For more in-depth searching go to view all 101 results from Patent Offices similar results
15.	Phase Interpolator Dunning, David S. / Abhayagunawardhana, Chamath / Drottar, Ken / Jensen, Richard S. / Glenn, Robert, UNITED STATES PATENT AND TRADEMARK OFFICE PRE- GRANT PUBLICATION, Jan 2003
	systems for clock recovery are describedof the phase interpolator of the presentto a remote clock recovery mechanism 17to reduce the interpolator output to veryc. a remote clock recovery mechanism comprising Full text available at patent office. For more in-depth searching go to view all 101 results from Patent Offices similar results
16.	COMPONENT TIMING RECOVERY SYSTEM FOR QAM KNUTSON, Paul, Gothard / RAMASWAMY, Kumar / McNEELY, David, Lowell,
	EUROPEAN PATENT, Jul 1999
r	control input of the interpolator so that the sampled signal produced by the interpolator represents the valuetolerances between the quadrature signals in a QAMexpense is desired. A clock recovery circuit for a demodulatorhaving in-phase and quadrature component processingestimator and an interpolator is described in EP-A
	Full text available at patent office. For more in-depth searching go to view all 101 results from Patent Offices similar results
17.	Phase-interpolator based PLL frequency synthesizer Chen, Chun-Ying / Le, Michael Q. / Wakayama, Myles, EUROPEAN PATENT, Sep

"clock recovery" AND interpolator AND quadrature results on scirus.com, for scientific i... Page 3 of 4

2003

...reference oscillating signals. The reference signals e.g. are in **quadrature** relationship and have approximately the same frequency. The document Larsson P.: "A 2-1600-MHz CMOS **Clock Recovery** PLL with Low- Vdd Capability", IEEE Journal of Solid-State... **Full text available at patent office. For more in-depth searching go to** LexisNexistiew all 101 results from Patent Offices similar results

■ 18. A direct-conversion CMOS radio receiver for high speed paging Chen, Zhiheng, Jan 2000

...included. The front-end consists of a differential LNA and a **quadrature** harmonic mixer. In the base-band, an AGC circuit provides...The demodulator is formed by a I-level zero-crossing **interpolator**, **clock recovery** circuits and decision logics. Main functions of the receiver...

Full text available from Hong Kong University of Science and Technology similar results

19. A Multi-gigabit CMOS Transceiver with 2x Oversampling Linear Phase Detection Vichienchom, Kasin, Feb 2003

...noise due to the bang-bang type phase detector in PLL-based **clock recovery** circuits has been analyzed using this model. The design...40 viii Figure 2.28 Phase **interpolator**...

Full text thesis available via NDLTD

view all 4 results from NDLTD similar results

20. Clock acquisition and tracking for burst communications

Frantzeskakis, Manolis / Aretos, Konstantinos, EUROPEAN PATENT APPLICATION, Jan 2001

...relates to the **clock recovery** process in burst...mapping such as **quadrature** amplitude modulation...clock, or by an **interpolator** device. Two variations...one concerns a **clock recovery** circuit for complex...of in-phase and **quadrature** components and the second one, a **clock recovery** circuit based...

Full text available at patent office. For more in-depth searching go to view all 101 results from Patent Offices similar results

:::fast

Results Pages: [<< Prev] 1 <u>2</u> <u>3</u> <u>4</u> <u>5</u> <u>6</u> <u>7</u> [Next >>]

back to top

<u>Downloads</u> | <u>Subscribe to News Updates</u> | <u>User Feedback</u> | <u>Advertising</u> <u>Tell A Friend</u> | <u>Terms Of Service</u> | <u>Privacy Policy</u> | <u>Legal</u>

Powered by FAST © Elsevier 2007





About Us

Newsroom

Advisory Board

Submit Web Site

Help

Contact Us

Basic Search

Advanced Search Preferences

			"clock recovery" A	ND interpolator AND	quadrature ANI	Search	
			☑ Journal sources	Preferred Web sources	✓ Other Web source	s Exact phrase	
	Sear	ched for::	:All of the words: "cl	ock recovery" AND into	erpolator AND quadra	ture AND "eye diagra	m"
		Found::	:30 total 0 journa	al results <u>15 preferre</u>	d web results 15 ot	her web results	
		Sort by::	:relevance <u>date</u>				
_		Save che	cked results Er	mail checked results	Export checked resu	ılts	Dic
	1.			2.5-3.125-Gb/s serial cuits, IEEE [PDF-34K		gh IO bandwidth	"cle int qu dia
		overcome power cor phase mix	traditional analog nsumptionPropose king interpolator is ww.ife.ee.ethz.ch/~	is based onanalog p g quadrature -phase ed Clock Recovery L s that itsignals. The vrodoni/download/loca	mixingcases. The loop A particularity of clock recovery lo	interpolator's of the quadrature	Re us for clo
	2.	Oct 200199 5.2.2 generation	n using phase inte <u>from</u> [http://mos.s	- CHIP [PDF-248K] torFigure 4.24: Rec rpolatorsSimplified stanford.edu/papers/s	model of the phase		phi phi phi phi
	3.	HIGH PER	FORMANCE INTER	- CHIP [PDF-249K]			<u>rin</u>
		99 5.2.3 generation	n using phase inte from [http://velox	torFigure 4.24: Rec rpolatorsSimplified .stanford.edu/papers/	model of the phase		SW Or Al
	4.		FORMANCE INTER	- CHIP [PDF-232K]			F
		generatio	n using phase inte r ww-vlsi.stanford.ed	torFigure 4.24: Rec rpolatorsSimplified u/papers/ss_thesis.pd	model of the phase		
	5.	E:\alevi\d Nov 2002		D Thesis\BinduThesis	<u>.pdf</u> [PDF-793K]		
			ns (58 ps peak-to-p	3.14 Measured (a) out leak) corresponding to			

view all 13 results from Patent Offices

similar results

Full text available at patent office. For more in-depth searching go to LexisNexis-

...multi-rate filter/interpolator (HB/VID) 20 which...under control of a clock recovery

loop, in a manner...In-phase (I) and quadrature phase (Q) baseband...constellation points using a quadrature synthesizer and complex...channel signals and quadraturephase (Q) channel...are subtended by an "eye" diagram illustrating the signal... Full text available at patent office. For more in-depth searching go to LexisNexisview all 13 results from Patent Offices similar results ☐ 18. DUAL MODE QAM/VSB RECEIVER JAFFE, Steven T. / LIU, Tian-Min / TAN, Loke, Kun, PATENT COOPERATION TREATY APPLICATION, May 2000 ...first tracking loop; a variable rate interpolator; an NTSC interference rejection filter...symbols characterized by in-phase and quadrature-phase portions separated in time by...to sample each of the in-phase and quadrature-phase portions of the complex signal at an in-phase sampling time and at a quadrature-phase sampling time separated by an... Full text available at patent office. For more in-depth searching go to LexisNexisview all 13 results from Patent Offices similar results 19. Technique for minimizing decision feedback equalizer wordlength in the presence of a DC Tan, Loke Kun / Liu, Tian-Min / Hung, Hing Ada T., UNITED STATES PATENT AND TRADEMARK OFFICE PRE-GRANT PUBLICATION, Sep 2001 ...multi-rate filter/interpolator (HB/VID) 20 which...under control of a clock recovery loop, in a manner...In-phase (I) and quadrature phase (Q) baseband...constellation points using a quadrature synthesizer and complex...channel signals and quadraturephase (Q) channel...are subtended by an "eye" diagram illustrating the signal... Full text available at patent office. For more in-depth searching go to LexisNexisview all 13 results from Patent Offices similar results **20.** Technique for minimizing decision feedback equalizer wordlength in the presence of a DC component Tan, Loke Kun / Liu, Tian-Min / Hung, Hing "Ada" T., UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, May 2001 ...multi-rate filter/interpolator (HB/VID) 20 which...under control of a clock recovery loop, in a manner...In-phase (I) and quadrature phase (Q) baseband...constellation points using a quadrature synthesizer and complex...channel signals and quadraturephase (Q) channel...are subtended by an "eye" diagram illustrating the signal... Full text available at patent office. For more in-depth searching go to LexisNexisview all 13 results from Patent Offices similar results

≕fast

Results Pages: [<< Prev] 1 2 [Next >>]

back to top

Downloads | Subscribe to News Updates | User Feedback | Advertising Tell A Friend | Terms Of Service | Privacy Policy | Legal

Powered by FAST © Elsevier 2007